REMARKS

This amendment is submitted in response to an Office Action mailed March 17, 2006. Applicant respectfully requests reconsideration of the subject application as amended herein.

Claims 1-41 remain in the present application.

Applicant has amended the specification to correct a previous undetected informality. No new matter has been entered.

The March 17, 2006 Office Action objected to claim 13, asserting that claim 13 "does not further limit the subject matter of the previous claim 1." Applicant respectfully disagrees. Claim 13 adds a "peripheral set" to the elements of claim 1. Claim 1 refers to a "peripheral set," but the peripheral set in claim 1 is not a required element. Specifically, claim 1 recites three elements in a processor - a memory element, an input element, and a comparison unit. The memory element is characterized in that it is to supply a setting "for use by a peripheral set," and the input element is characterized in that it is to receive a setting "from the peripheral set," but the peripheral set itself is not required to infringe claim 1, nor is any interaction with the peripheral set required to infringe claim 1. That is, claim 1 requires only a processor, by itself and inactive, so long as the processor includes a memory element, an input element, and a comparison unit capable of the interactions described in claim 1. Put another way, claim 1 can be infringed even in the absence of the "peripheral set." Claim 13, on the other hand, requires both the processor of claim 1 and the peripheral set (a processor plus a chipset, for instance). Therefore, Applicant respectfully requests that the objection to claim 13 be withdrawn.

The March 17, 2006 Office Action rejected claim 16 under 35 U.S.C. § 112, first paragraph, asserting that the "specification and figures disclose that the clock rate feedback unit is a separate circuit" rather than "a circuit within the clock generator" or "a circuit within the processor," as claimed in claim 16. Applicant respectfully disagrees. At page 6, line 29 to page 7, line 2, the specification states,

> Furthermore, although feedback output unit 145 is shown as part of memory controller hub 107, it can be located in any number of other places. For example, unit 145 could be within clock generator 115, within processor 100, a separate component in peripheral set 175, etc.

Applicant respectfully submits that anyone skilled in the art can implement a "clock rate feedback unit" as claimed and described just as easily as a separate circuit or incorporated into other components, including a processor or clock generator. Therefore, Applicant respectfully requests that this rejection of claim 16 be withdrawn.

In the March 17, 2006 Office Action, claims 1-5, 7, 12, 14-15, 18-32, 35, 36, and 38-41 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,385,735 issued to Wilson et al. (hereinafter "Wilson"). As discussed below, Applicant respectfully submits that claims 1-5, 7, 12, 14-15, 18-32, 35, 36, and 38-41 are not anticipated by Wilson. For example, claim 1 includes:

> An apparatus comprising:
> a memory element in a processor to supply a configured clock rate setting for use by a peripheral set;
> an input element in the processor to receive a feedback clock rate setting from the peripheral set; and

> a comparison unit in the processor to compare the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor.

In other words, the processor in claim 1 can tell a peripheral set what the clock setting is for the processor, and the peripheral set is expected to echo that clock setting back. If the feedback is not the expected echo (less-than-or-equal-to, for instance), the comparison unit can detect over-clocking.

In contrast, Wilson describes setting the clock rate for a processor by setting "jumpers" on a motherboard (Wilson: col. 2, lines 51-55). Then, the motherboard uses a set of frequency selection signals to tell the processor what the clock rate is (Wilson: col. 2, lines 55-58), rather than the processor telling the motherboard what clock rate to use. In other words, in Wilson, the motherboard cannot "echo" a clock rate setting back to the processor because the processor does not first supply clock rate information for the motherboard.

Therefore, Applicant respectfully submits that Wilson does not suggest, disclose, or enable "a memory element in a processor to supply a configured clock rate setting for use by a peripheral set," as claimed in claim 1.

Thus, for at least the reasons discussed above, Applicant respectfully submits that claim 1 is patentable over Wilson.

Applicant submits that the reasoning presented above with respect to claim 1 similarly applies to claims 2-5, 7, 12, 14-15, 18-32, 35, 36, and 38-41. Thus, for at least the reasons discussed above, Applicant respectfully submits that claims 2-5, 7, 12, 14-15, 18-32, 35, 36, and 38-41 are likewise patentable over Wilson.

In the March 17, 2006 Office Action, claims 6, 17, and 37 were rejected under 35 U.S.C. § 103 as being unpatentable over Wilson. Applicant respectfully submits that the reasoning presented above with respect to Wilson similarly applies to claims 6, 17, and 37. Thus, for at least the reasons

discussed above, Applicant respectfully submits that claims 6, 17, and 37 are likewise patentable over Wilson.

In the March 17, 2006 Office Action, claims 8 and 33 were rejected under 35 U.S.C. § 103 as being unpatentable over Wilson in view of U.S. Patent No. 6,691,242 issued to Pollock et al. (hereinafter "Pollock"). Applicant respectfully submits that the reasoning presented above with respect to Wilson similarly applies to claims 8 and 33. Pollock was cited for teaching "outputting an over-clocking detection signal from the processor." Assuming purely for the sake of argument that the Office Action is correct with respect to the teachings of Pollock, Applicant respectfully submits that Pollock fails to cure the deficiencies of Wilson as discussed above. Therefore, Applicant respectfully submits that claims 8 and 33 are patentable over Wilson in view of Pollock.

In the March 17, 2006 Office Action, claims 9-11 and 34 were rejected under 35 U.S.C. § 103 as being unpatentable over Wilson in view of U.S. Patent No. 6,073,249 issued to Watabe et al. (hereinafter "Watabe"). Applicant respectfully submits that the reasoning presented above with respect to Wilson similarly applies to claims 9-11 and 34. Watabe was cited for teaching "use of a tri-state unit and a logic AND." Assuming purely for the sake of argument that the Office Action is correct with respect to the teachings of Watabe, Applicant respectfully submits that Watabe fails to cure the deficiencies of Wilson as discussed above. Therefore, Applicant respectfully submits that claims 9-11 and 34 are patentable over Wilson in view of Watabe.

In conclusion, Applicant respectfully submits that claims 1-41 are now in a condition for allowance, and Applicant respectfully requests allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 50-0221.

Respectfully submitted,

INTEL CORPORATION

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